30.5 A Self-Calibrated On-chip Phase-Noise-Measurement Circuit with -75dBc Single-Tone Sensitivity at 100kHz Offset

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PLLs perform a variety of timing-related functions such as frequency synthesis and CDR. As the process technology scales down and system requirements such as RF frequency and modulation bandwidth scale up, phase noise in signal sources becomes one of the limiting specifications in communication circuits [1]. For example, in SONET CDR circuits where multiple PLLs are cascaded, an accurate prediction of the jitter frequency response is critical in reducing the impact of jitter peaking by measuring it and adaptively tuning the PLL response. Recently, on-chip time-domain jitter-measurement techniques using direct time-interval measurement and auto-correlation have been proposed [3, 4]. On-chip time-interval-based jitter-measurement methods are usually limited by the purity of the reference clock [2] and/or gate-delay resolution of the given process technology [2-4]. While it is well known that measuring phase noise in the frequency domain is the most accurate method for computing jitter, it has been limited so far to off-chip methods utilizing spectrum analyzers or specialized measurement equipment.

This paper reports a frequency-domain on-chip phase-noise measurement circuit accurately measuring phase noise up to 2MHz offset from carrier with single-tone (ST) sensitivity of -75dBc at 100kHz. The proposed circuit also has a built-in auto-calibration scheme that guarantees quadrature relationship at the 2 inputs of the mixer, operating the measurement circuit at its highest sensitivity point.

Figure 30.5.1 shows the block diagram of the proposed on-chip phase-noise measurement module showing spectral content for a typical clock phase noise and an ST narrowband FM test input. The circuit uses a delay-line and mixer-based frequency discriminator to convert short-term phase deviations in a signal source to baseband voltage fluctuations. The correlation signal is then low-pass filtered (LPF) to reject the out-of-band frequency components and then gained up using a baseband LNA (BBLNA). The output of the system is either directly analyzed in analog domain or digitized for further FFT processing. The phase-noise profile of the clock-under-test (CUT) can be calculated at a given frequency offset by estimating the power-spectral-density (PSD) of the output voltage signal.

Circuit-level block diagram of the delay discriminator module is shown in Fig. 30.5.2. The CUT signal is divided into 2 signal paths; the first part is passed through a variable delay line with its delay controlled by the on-line feedback-calibration loop. The calibration circuit is comprised of a DC-offset comparator, a digital integrator, and a supply-regulated delay-line. Under ideal quadrature conditions between the CUT signal and its delayed version, DC offsets at the output of the signal chain is minimum and instantaneous phase fluctuations at the mixer input are accurately sensed and converted to voltage fluctuations. The proposed calibration loop ensures this condition by continuously monitoring the DC offset at the output of the module, maximizing the gain and sensitivity of the phase-noise measurement system under PVT variations. The delay line consists of an array of cascaded inverters that are optimized for low phase noise. A single-ended to differential circuit (S-to-D) is used to convert the output of the delay line to a differential signal that drives the RF port of the mixer. The second path of the CUT signal is converted to a differential signal before it directly drives the LO port of the switching mixer. The output of the mixer is then amplified and filtered using a BBLNA that is combined with a single-pole LPF.

Figure 30.5.3 shows the combined circuit schematic for the mixer, BBLNA and LPF. The fully differential CMOS double-balanced mixer cell resembles a MOSFET-C LPF structure where the mixing operation is achieved by modulating the conductance of a CMOS transmission gate operating in triode region. To allow a phase-noise measurement bandwidth of 20MHz while suppressing higher frequency mixing products, the mixer output is filtered using a first-order pole in the feedback of the BBLNA with a nominal bandwidth of 26MHz. The BBLNA is based on a 2-stage fully differential amplifier with the input stage having a half-side cascoded active load. A continuous-time CMFB circuit is used for common-mode control while driving an ADC or a differential buffer. The combined mixer/BBLNA has a conversion gain of 4.7dB and 3rd-harmonic distortion of -53dB. The total noise of the phase-discriminator block is dominated by the $1/f$ noise of the mixer. This is illustrated by comparing the input referred noise contribution of all the major building blocks in the lower part of Fig. 30.5.4.

The VCDL is realized with a chain of 100 inverters. The supply of the VCDL is adjusted with the calibration feedback to vary the line delay and modulate the phase difference between the CUT and delay output paths. The device sizes for the inverters are optimized to minimize the close-in phase-noise impact of the delay line on the propagating signal. While increasing the number of cascaded inverters adds more delay through the line improving the accuracy of the measurement system, it also results in degrading the phase noise of the propagating signal. The trade-off between phase noise and line delay at the output of the VCDL is shown in the upper part of Fig. 30.5.4. The phase-noise contribution of the VCDL is designed to be below -120dBc/Hz at 10kHz offset. In the delay-discriminator case, the deviation from the quadrature condition is amplified by the line delay time that results in significantly larger DC offset and amplitude errors compared to a standalone mixer, as shown in Fig. 30.5.5. The optimum measurement point refers to the minimum DC offset at the discriminator output, as shown in Fig. 30.5.5. As a worst-case example, with a 2.5% deviation from quadrature, a 20ns delay can nullify the accuracy of the phase-noise measurement circuit.

The noise floor and linearity of the phase-noise measurement circuit is determined by measuring its response to a 1GHz carrier signal modulated with an ST narrowband FM signal. As shown in Fig. 30.5.1, the phase noise measured at the discriminator output is expressed as the sideband to carrier ratio of the FM-modulated CUT signal. The ST linearity and absolute accuracy of the module is shown in Fig. 30.5.6. The equivalent phase-noise sensitivity in dBc/Hz is also plotted in Fig. 30.5.6. The phase-noise sensitivity is extracted by integrating the ST results over a window of 3 consecutive measurement points and averaging the output over the window bandwidth. The proposed technique represents an on-chip phase-noise measurement circuit that can attain an ST sensitivity of -75dBc at 100kHz offset from the carrier. The phase-noise measurement module has an equivalent sinusoidal jitter sensitivity of 113fs-peak at 100kHz jitter frequency. The module is fabricated in a 0.25μm CMOS process and it occupies $1.4\times0.35mm^2$ (Fig. 30.5.7).

References:

[1] Cascaded PLL Design for a 90nm CMOS High Performance Microprocessor," *ISSCC Dig. Tech. Papers*, pp. 422- 423, Feb., 2003.

[2] M. Takamiya, H. Inohara, M. Mizuno, "On-chip Jitter-Spectrum-Analyzer for High-Speed Digital Designs," *ISSCC Dig. Tech. Papers*, pp. 350- 351, Feb., 2004.

[3] M. Ishida, K. Ichiyama, T.J. Yamaguchi, et. al. "A Programmable On-chip Picosecond Jitter-Measurement Circuit Without a Reference-Clock Input," *ISSCC Dig. Tech. Papers*, pp. 512 -513, Feb., 2005.

[4] K. Nose, M. Kajita, M. Mizuno,"A 1ps-Resolution Jitter-Measurement Macro Using Interpolated Jitter Oversampling," *ISSCC Dig. Tech. Papers*, pp. 520-521, Feb., 2006.

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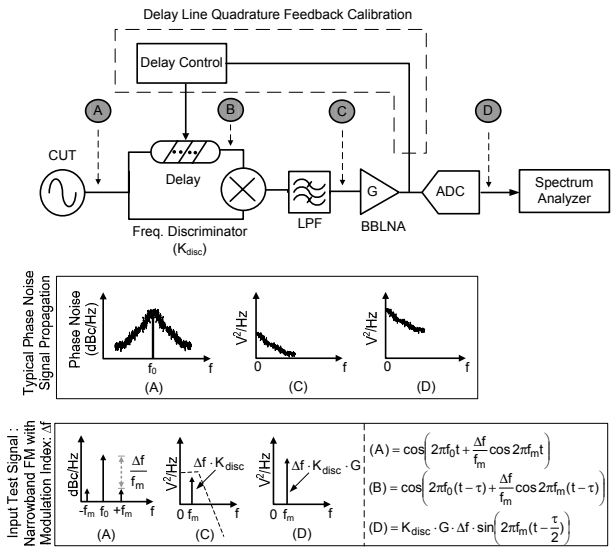


Figure 30.5.1: Architectural block diagram with associated measurement concept.

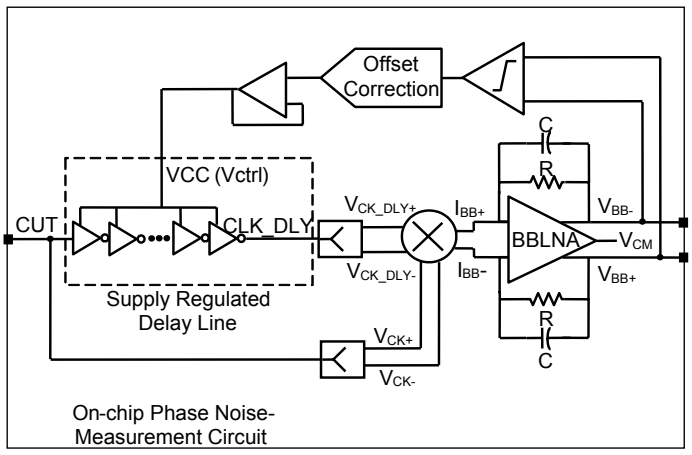


Figure 30.5.2: Circuit diagram of the self-calibrated measurement module.

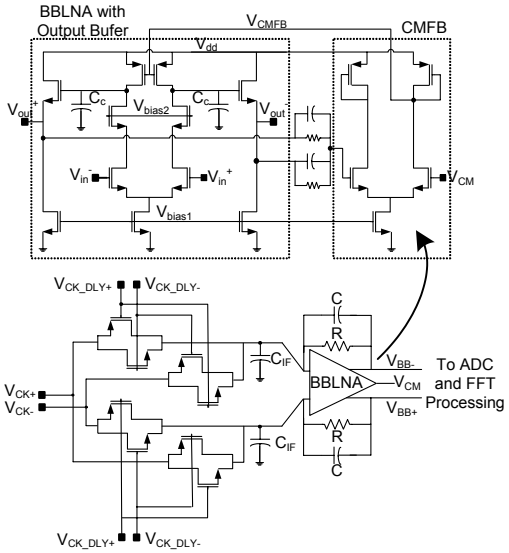


Figure 30.5.3: Switching mixer, BBLNA and LPF.

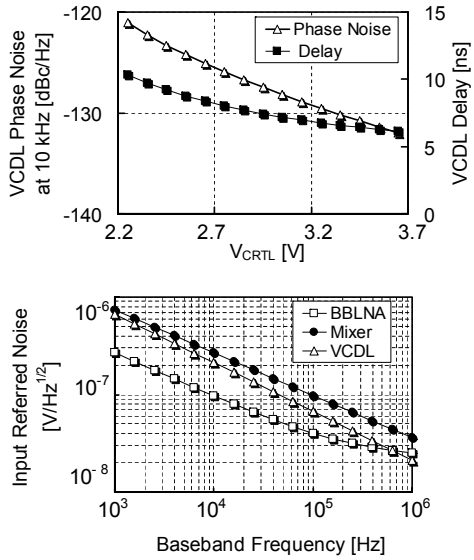


Figure 30.5.4: Input referred noise contribution of the VCDL, BBLNA and mixer.

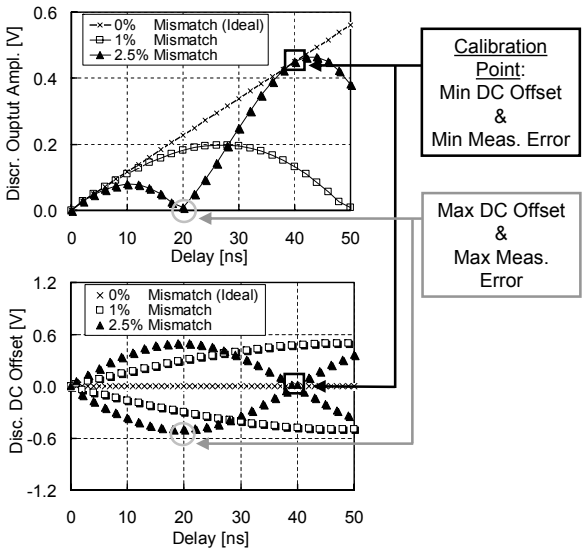
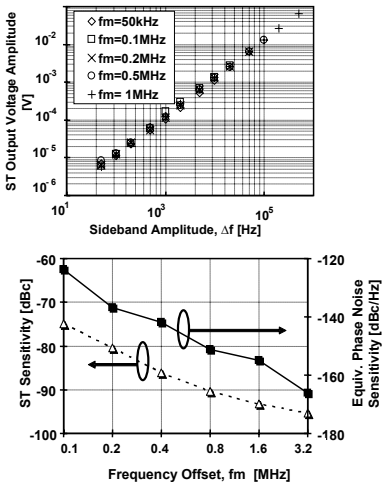


Figure 30.5.5: Discriminator amplitude error and DC offset vs. delay.



Sideband Ampl.:Δf	Max Linearity Error
50kHz	0.45dB
100kHz	1.36dB
200kHz	1.51dB
500kHz	0.55dB
1MHz	0.87dB

Freq. Offset; f_m	ST Measured Error vs. Theoretical
50kHz	1.55dB
100kHz	2.86dB
500kHz	1.41dB
2MHz	2.72dB

Figure 30.5.6: Linearity and sensitivity measurement results.

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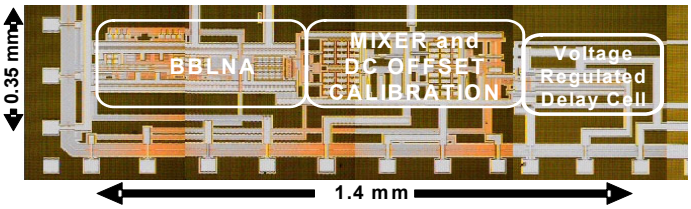

Figure 30.5.7: Die micrograph.

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